**IN THE CLAIMS:**

None of the claims have been amended herein. All of the pending claims 17-26 and 46-50 are presented below. This listing of claims will replace all prior versions and listings of claims in the application.

Claims 1-16 are canceled.

17. A semiconductor processing method of forming an electrical contact structure for an active area on a semiconductor wafer, the method comprising the following steps:

providing a pair of conductive runners on a semiconductor wafer, individual conductive runners having sides;

providing an insulative layer on the mutually adjacent sides of the conductive runners, the insulated mutually adjacent sides of adjacent conductive runners being spaced a selected distance apart;

providing an active area between the insulated mutually adjacent sides of conductive runners;

providing a layer of first oxide to a selected thickness over the active area and conductive runners, the first oxide layer selected thickness being less than one-half the selected distance between the insulated sides of adjacent conductive runners;

providing a first insulating layer having a planarized upper surface atop the first oxide layer, the first layer of insulating material being selectively etchable relative to the first oxide;

patterning the first insulating layer for definition of a first contact opening therethrough to the active area;

etching the patterned first insulating layer selectively relative to the first oxide layer to define the first contact opening therethrough, the first contact opening having an aperture width at the first insulating layer planarized upper surface, the aperture width being greater than the selected distance between the insulated sides of adjacent conductive runners:

etching the first oxide layer within the first contact opening to expose the active area; and

providing a conductive plug of within the first contact opening over the exposed active area.

18. A semiconductor processing method according to claim 17 wherein the step of providing a plug of conductive material comprises:

providing a layer of conductive material over the first insulating layer and within the first contact opening over the exposed active area; and

polishing the wafer to remove the conductive layer from the first insulating layer planarized upper surface and to define the conductive plug within the first contact opening, the plug having an upper surface slightly below the first insulating layer planarized upper surface.

19. A semiconductor processing method according to claim 17 further comprising:

providing a second insulating layer and the conductive plug; and

patterning and etching the second insulating layer to form a second contact opening to expose the conductive plug.

20. A semiconductor processing method according to claim 19 further comprising etching the second insulating layer with an etchant selective to both the first insulating layer and the conductive plug.

21. A semiconductor processing method according to claim 19 further comprising:

forming the first insulating layer of a nitride;

forming the conductive plug of polysilicon; and

etching the second insulating layer with an etchant selective to both the nitride insulating layer and the polysilicon plug.

22. A semiconductor processing method of forming an electrical contact structure for an active area on a semiconductor wafer, the method comprising the following steps:

providing a pair of conductive runners on a semiconductor wafer, individual conductive runners having sides;

providing an insulative layer on the mutually adjacent sides of the conductive runners, the insulated mutually adjacent sides of adjacent conductive runners being spaced a selected distance apart;

providing an active area between the insulated mutually adjacent sides of conductive runners;

providing a layer of first oxide to a selected thickness over the active area and conductive runners, the first oxide layer selected thickness being less than one-half the selected distance between the insulated sides of adjacent conductive runners;

providing a first insulating layer having a planarized upper surface atop the first oxide layer, the first insulating layer being selectively etchable relative to the first oxide, said step performed by,

providing a conformal first layer of insulating material atop the first oxide layers; and

polishing the wafer to planarize the first insulating layer upper surface;

patterning the first insulating layer for definition of a first contact opening therethrough to the active area;

etching the patterned first insulating layer selectively relative to the first oxide layer to define the first contact opening therethrough, the first contact opening having an aperture width at the first insulating layer planarized upper surface, the aperture width being greater than the selected distance between the insulated sides of adjacent conductive runners;

etching the first oxide layer within the first contact opening to expose the active area; and

providing a conductive plug within the first contact opening over the exposed active area.

23. A semiconductor processing method for making electrical contact with an active area on a semiconductor wafer comprising the steps of:

providing a pair of conductive runners on a semiconductor wafer, individual conductive runners having a top and sides;

providing insulative spacers on mutually adjacent sides of the runners, the insulative spacers being spaced a selected distance apart at a selected location on the wafer;

providing an active area between the conductive runners at the selected location;

depositing a first oxide layer over the wafer to a thickness from about 100 to 1,000 Angstroms, the first oxide layer having an upper surface defining a highest elevational location above the active area;

providing a nitride layer having an upper surface over the first oxide layer to a selected thickness, the nitride layer upper surface defining a lowest elevational location above the active area which is elevationally higher than the highest elevational location of the first oxide layer, the nitride being selectively etchable relative to the first oxide;

planarizing an upper surface of the nitride layer to a first elevational height above the active area, the first elevational height being higher than the highest elevational location of the first oxide layer upper surface;

patterning the nitride layer for definition of a first contact opening therethrough to the active area;

etching the patterned nitride layer selectively relative to the first oxide layer to define the first contact opening therethrough, the first contact opening having an aperture width at the nitride layer upper surface which is greater than the selected distance between the insulative spacers at the mutually adjacent sides of the conductive runners;

etching the first oxide layer within the first contact opening to expose the active area;

providing a polysilicon plug within the first contact opening over the exposed active area to a second elevational height; and

depositing a second oxide layer over the nitride layer and the polysilicon plug.

24. A semiconductor processing method according to claim 23 wherein the step of planarizing the nitride layer comprises polishing the wafer to planarize the nitride layer.

25. A semiconductor processing method according to claim 23 wherein the step of providing a polysilicon plug comprises:

providing a layer of polysilicon over the nitride layer and within the first contact opening over the exposed active area; and

polishing the wafer to remove the polysilicon layer from the nitride layer upper surface and to define a polysilicon plug within the first contact opening.

26. A semiconductor processing method according to claim 23 further comprising etching the second oxide layer by an etchant selective to both the nitride layer and the polysilicon plug.

Claims 27-45 are canceled.

46. A method of providing electrical communication with a transistor including a source/drain, said method comprising:

providing a conductor over said source/drain that extends upward and is laterally surrounded by a first layer of insulation;

providing a second layer of insulation over said first layer of insulation, wherein said second layer of insulation is higher than said conductor and exposes said conductor; and

allowing electrical communication with said source/drain only by way of said conductor.

47. The method in claim 46, wherein said step of providing a conductor comprises providing a plug.

48. A method of processing a device comprising a transistor, said method comprising:

providing a plug in electrical communication with said transistor;

providing a conductive material in electrical communication with said plug; and

providing an insulating layer lateral to said conductive material, wherein said step of providing an insulating layer occurs before said step of providing a conductive material.

49. The method in claim 48, further comprising a step of providing a first insulating layer over said transistor; and wherein said step of providing an insulating layer lateral to said conductive material comprises providing a second insulating layer over said first insulating layer.

50. The method in claim 49, wherein said step of providing a conductive material is discrete from said step of providing a plug.